Exploring Transistor Sizing for Radiation Hardening in 2:1 Multiplexer Designs

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Abstract—**The evolution of circuit manufacturing technology has allowed for greater integration of these components. To achieve this, the dimensions of the transistors have been reduced, as well as their supply voltage, significantly impacting the reliability of these circuits. In this context, transient faults are recognized as a major threat to electronic devices. Multiplexers are used in digital circuits, acting as a data selector switch, therefore, a fundamental circuit for numerous logic applications. The objective of this work is to analyze the robustness of six different 2:1 multiplexer designs, considering the area of the largest circuit. For this, the sensitive regions were analyzed, and a transistor sizing technique was applied according to the susceptibility of each circuit. The circuit analysis was performed by identifying the sensitive nodes in the transistor arrangement, and based on this information, electrical simulations were carried out to determine the minimum critical charge value required to cause a fault. With these values, the critical charge was calculated. The new sizing explored showed gains of up to 2x in the multiplexer robustness. This result demonstrates the importance of exploring radiation hardening techniques.**

Index Terms—**Multiplexer 2:1, Single Event Transient, Radiation Faults, Reliability**

I. INTRODUCTION

The Very Large Scale Integration (VLSI) technology refers to the integration of thousands of MOS transistors on a single chip, bringing more functionality to new electronic devices. In this context, reductions on transistors dimensions and the voltage used for their operation have significantly affected the reliability of these devices [1]. Therefore, in scenarios where circuits are exposed to radiation, such as in space equipment, airplanes, medical equipment, among others, robustness is fundamental for the reliability of their operations and the safety of people. Furthermore, the reduction in the operating voltage of these circuits has made not only aerospace devices critical, but also circuits that operate at terrestrial level [2].

A 2:1 multiplexer, shortened to "MUX 2:1" , is a combinational logic circuit designed to select, through the selector "S", only one data input, A or B, and send it to the output. The multiplexer can have its behavior simplified as a digital switch, having 2^n inputs, an *"n"* bit selector and an output. Furthermore, they are widely used in arithmetic circuits, and mainly in larger projects to determine the data path in complex computer systems.

Therefore, this paper performs a radiation robustness analysis for six 2:1 multiplexer designs. To this end, a mapping of sensitive active areas, called sensitive nodes, was carried out at the transistor arrangement level. Subsequently, electri-

cal simulations of Single Event Transient (SET) faults were carried out. In the section II, the concepts necessary for a full understanding of this work are reviewed. The section III describes the methods used to perform the robustness analysis of the multiplexer circuits, the description of the current command and the equations used to obtain the collected charge values. In the IV section, the results are discussed in relation to the robustness of the selection and output nodes of the designs. Finally, in the section V, the conclusion of this work and proposals for future work are presented.

II. BACKGROUND

Single Event Effects (SEE) are caused when highly energetic particles present in the natural space environment (e.g., protons, neutrons, alpha particles, or other heavy ions) strike sensitive regions of a circuit [3] [1]. Depending on several factors (such as incidence angle, particle energy, technology used, type of transistor impacted, among others) a particle can cause anything from no observable effect, a transient fault in an operation or cause permanent damage in the circuit. Thus, SEEs are classified as non-destructive (Soft Errors) or destructive (Hard Errors) [4] [5].

The SET is a type of Soft Errors. They are characterized as a transient disturbance in the voltage of combinational circuits, which can propagate and induce an error in a memory element [5]. They are caused by the impact of a highly energetic particle on an reverse-biased PN region of the circuit [6]. The effect of this fault depends on the amount of energy released, the angle of incidence, particle energy, device technology, device supply voltage and the type of transistor impacted [7]. If the collision occurs at a sensitive node of a PMOS transistor, there will be a 010 pulse in the node. If the particle hits a reverse-biased PN region of an NMOS transistor, a 101 pulse will occur in the node. Fig. 1 shows the behavior of a SET fault in a sensitive region of the circuit.
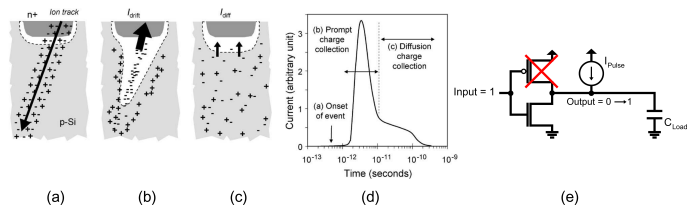

Fig. 1. Stages of incidence of a particle in a PN region [8].

Fig. 1 (a) shows the moment when a particle collides with a sensitive node of a transistor, causing electron-hole pairs. Fig. 1 (b) shows the path of the unbalanced particle passage, resulting in a temporary funnel-shaped deformation (funneling effect). As a result, there is a high transient current at the node. Fig. 1 (c) shows the diffusion process that collects the resulting carriers [8]. The graph of the transient current generated with the incidence of the particle on the transistor is shown in Fig. 1 (d). The Fig. 1 (e) shows a simulation of a SET fault at the output of an inverter. In this case, the current source simulates the electrical behavior of a SET, generating a transient pulse 010 at the output.

III. METHODOLOGY

In this paper, a proposal for optimization of sizing critical regions in 2:1 multiplexer circuits is carried out under a standard area cost. The designs were chosen from the works of [9] and [10], which discussed aspects of speed, power consumption, delay and area using different logic styles. The circuits analyzed in this work are presented in the Fig. 3. To simulate circuits, the Planar CMOS technology and the 32 nm High Performance (HP) predictive model were used [11]. The format used was the SPICE netlist, and the simulation was done in NGSPICE [12] with a nominal voltage of the technology 0.9V. The methodology was organized in three stages, as can be seen in Fig. 2.
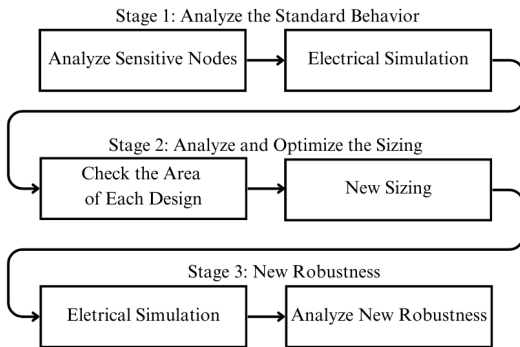

Fig. 2. Methodology Flowchart.

A. Stage 1: Analyze the standard behavior

To determine the standard radiation robustness characteristics of each circuit, the Logical Effort technique was initially used. For the length, the smallest of the technology was considered and the size of width (W) 70 nm was considered for NMOS and 140 nm for PMOS. Next, an analysis was performed on each design to identify the sensitive nodes. For this, a sensitive node was defined as any reverse-biased PN junctions that have a conductive path to the circuits output [6]. The potentially sensitive nodes of each design are identified with a black circle in Fig. 3.

In this work, the selector input is identified as "S" in the circuits of Fig. 3, and its internal node is named n1. The only design that does not have this node is the Fig. 3 (D),

as this design performs selection through direct biasing of the transistors.

With the information on the sensitive nodes, the next step was to carry out electrical simulations to identify the impact of the SET fault on the designs. The SET faults are modeled as a double exponential current pulse originating in the node struck by the charged particle [13]. To perform electrical simulations considering a real environment, the Design Under Test (DUT) was created, illustrated in Fig. 4. In this environment, the circuit is simulated considering input and output capacitance (Fan-in and Fan-out).

To analyze a SET fault, the logical state in normal operation of each sensitive node was first identified. Next, the current source was inserted into the reverse-biased transistor node, as indicated in Fig. 1 (e). When applying the transient pulse, it was possible to observe its propagation at the circuit output. To be classified as a fault, the pulse needed to exceed 50% of the nominal VDD value (i.e., 0.45V).

To perform the simulation, some parameters of the command need be declared: current source connection nodes, initial value of the current - I(t), rise delay time TD1, fall delay time TD2, rise time constant TAU1 ($T\beta$) and fall time constant TAU2 ($T\alpha$).

$$I[nome]\ nodo1\ nodo2\ EXP\ (I1\ I2\ TD1\ TAU1\ TD2\ TAU2)$$

With the critical current value obtained from the simulation I(t), it was possible to calculate the critical charge values according to equation 1 [13]. The constants $T\alpha$ and $T\beta$ are, respectively, 164 ps and 50 ps.

$$Qcrit = I(t) \times (T\alpha - T\beta) \qquad (1)$$

The result of this first stage indicated that the n1 and the output are the most critical regions of the multiplexers. Based on this finding, a new sizing was done in order to increase the robustness of these regions.

B. Stage 2: Analyze and optimize the sizing

Considering the results of Step 1, the total area was estimated by summing the size of all transistors in each design. The largest circuit was the (E) AND, thus defining it as the standard area cost. Afterwards, a new resizing was performed, increasing the size of Wp and Wn of the transistors, as highlighted in Fig. 3, in order to improve the robustness of node n1 and the output. The results of the area calculation before and after the optimization of resizing are presented in Table I.

TABLE I
ESTIMATED AREAS OF EACH DESIGN IN EACH SIZING TECHNIQUE

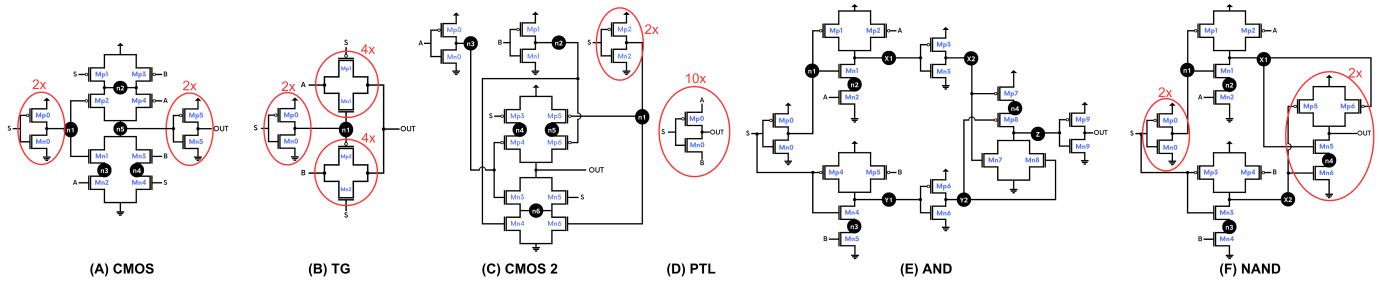| Design	Area 1 (nm)	Area 2 (nm)	Increase (%)
(A) CMOS	2100	2520	20,00%
(B) TG	630	2100	233,33%
(C) CMOS 2	2310	2520	9,09%
(D) PTL	210	2100	900,00%
(F) NAND	1890	2660	40,74%
(E) AND	2660	-	0,00%

Fig. 3. Multiplexers 2:1 Designs.

Fig. 4. Design Under Test.

C. Stage 3: New Robustness

With the new sizing of the circuits, new electrical simulations were carried out to analyze the new robustness behavior. The simulations were performed following the same criteria as Stage 1.

IV. RESULTS

In this section, the results of optimizing the size of multiplexer designs will be discussed. Table IV is organized in six columns, and presents summarizes the critical charge for all designs evaluated in this work. The first column indicates the design of the multiplexer, the second the critical nodes that have been resized, the third shows the input vector (considering S, A and B). The fourth column shows the critical charge value at the first resizing (as described in Stage 1 in the III section) and the fifth column shows the critical load result with the circuit resized (as described in Stage 2 in the III section). Finally, the last column shows the percentage increase in robustness for each input vector.

Designs that use pass transistors show better results in terms of power consumption and area optimization [14]. In this study, the multiplexers that use pass transistors are those in Fig. 3 (B) and (D). These designs have increased their area the most compared to the others, as can be seen in Table I.

Looking at the TG design (B), you can see that the critical charge on the output node is constant among the input vectors. However, this is not the case for node n1. Node n1 has a large difference in susceptibility between the input vectors, due to competitive behavior when inputs A and B have different logic values.

When analyzing design (D) PTL, it can be seen that it was the design that achieved the greatest increase in the percentage of robustness. However, although the transistors were 10x larger, there was no considerable increase in the absolute value of the critical charge. This behavior occurs because in

this case, the simulation environment considers that the input signals come from buffers that are not being analyzed (they serve as simulated input capacitance and are not altered in the sizing).

Designs using Static CMOS show better results in terms of radiation robustness and efficiency. These designs have had their selection and output nodes strengthened with the new sizing. The Fig. 3 (A) CMOS design increased its total area by 20% by doubling the size of the circuit's Select input and output inverters. As a result, the robustness of these nodes doubled for all input vectors, as can be seen in Table IV.

The Fig. 3 (C) CMOS 2 design was the only circuit that could not be optimized at the output, as can be seen in Fig. 3. However, in its critical input vector 101 for n1 node, its robustness was increased by more than 107%. The NAND, Fig. 3 (F) design, with a 40% increase in area, was the design that showed the best gains in terms of robustness. With the new sizing, the output, n1 and n4 nodes became twice as robust.

In order to summarize the results obtained with the new sizing, Fig. 5 shows the critical charge results for output and n1 nodes of each design. It can be seen that all the designs showed improvements in the robustness of the output node, except for the CMOS2 design. Therefore, by exploring the area of the largest design, considerable gains in robustness can be made by analyzing other design possibilities.
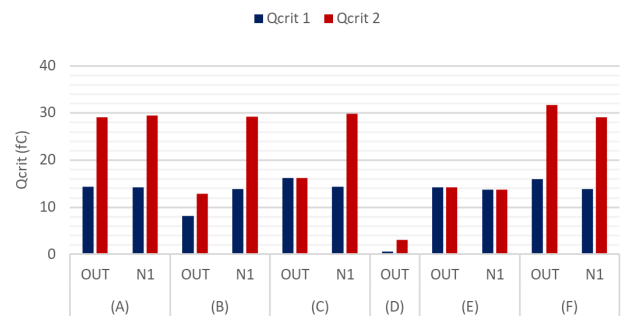

Fig. 5. Critical charge of each sensitive node.

V. CONCLUSION

This paper presented a comparative analysis of the robustness to transient faults of six 2:1 multiplexer designs,

Design	Nodes	Input Vector	Qcrit 1 (fC)	Qcrit 2 (fC)	Increase (%)
(A) CMOS	OUT	000	14.364	29.070	102.38%
		001	14.364	29.184	103.17%
		010	17.784	35.910	101.92%
		011	17.784	35.910	101.92%
		100	14.364	29.070	102.38%
		101	17.784	35.910	101.92%
		110	14.364	29.184	103.17%
		111	17.784	35.910	101.92%
	N1	010	17.898	36.480	103.82%
		011	18.240	37.278	104.38%
		110	14.250	29.526	107.20%
(B) TG	OUT	000	8.208	12.882	56.94%
		001	8.208	12.882	56.94%
		010	8.664	13.680	57.89%
		011	8.664	13.680	57.89%
		100	8.208	12.882	56.94%
		101	8.664	13.680	57.89%
		110	8.208	12.882	56.94%
		111	8.664	13.680	57.89%
	N1	001	18.012	37.050	105.70%
		010	35.340	72.162	104.19%
		101	13.908	29.184	109.84%
		110	20.292	37.620	85.39%
(C) CMOS 2	OUT	000	20.976	20.976	0.00%
		001	16.188	16.188	0.00%
		010	16.872	16.872	0.00%
		011	17.100	17.100	0.00%
		100	20.748	20.748	0.00%
		101	17.214	17.214	0.00%
		110	16.188	16.188	0.00%
		111	17.328	17.328	0.00%
	N1	001	18.810	38.532	104.85%
		101	14.364	29.868	107.94%
		111	14.592	30.210	107.03%
(D) PTL	OUT	000	684	3.078	350.00%
		001	684	3.078	350.00%
		010	8.436	15.846	87.84%
		011	8.436	15.846	87.84%
		100	8.094	14.250	76.06%
		101	570	3.534	520.00%
		110	8.094	14.250	76.06%
		111	570	3.534	520.00%
(E) AND	OUT	000	14.250	14.250	0.00%
		001	14.250	14.250	0.00%
		010	17.784	17.784	0.00%
		011	17.784	17.784	0.00%
		100	14.250	14.250	0.00%
		101	17.784	17.784	0.00%
		110	14.250	14.250	0.00%
		111	17.784	17.784	0.00%
	N1	010	18.126	18.126	0.00%
		011	18.126	18.126	0.00%
		110	13.794	13.794	0.00%
(F) NAND	OUT	000	15.960	31.692	98.57%
		001	15.960	31.692	98.57%
		010	17.784	36.024	102.56%
		011	17.784	36.024	102.56%
		100	15.960	31.692	98.57%
		101	18.012	36.480	102.53%
		110	15.960	31.692	98.57%
		111	18.012	36.480	102.53%
	N1	010	18.126	37.278	105.66%
		011	18.126	37.278	105.66%
		110	13.908	29.070	109.02%
	N4	101	17.784	36.024	102.56%
		111	17.784	36.024	102.56%

exploring a sizing strategy to reinforce the critical nodes of each design. To do this, it was necessary to understand the standard behavior of the circuits and identify the critical nodes that needed to be strengthened. The designs in pass transistor logic style were the ones that increased their transistors the most, however, this was not enough to obtain good robustness in the output node of these circuits. The (C) CMOS design was the only one that did not improve its output, as it had already reached its area limit. The designs that showed the best results were the (A) CMOS and (F) NAND designs, with double the robustness being observed. With this, the results show the importance of exploring transient fault mitigation techniques in different multiplexer designs, in the search for the best configuration. Future work includes layout analysis of the area impact of this sizing on these designs.

ACKNOWLEDGMENT

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